ADDRESS QUEUE

ADDRESS QUEUE

OUTPUT#1

OUTPUT#2

OUTPUT#4

OUTPUT#4

OUTPUT#4

OUTPUT#4

OUTPUT#4

#1

#2

#3

CIRCUIT

#4

MUX

JOHN DESTINATION

OUTPUT PORTS

OUTPUT PORTS

#1

#2

#3

#4

DEMUX

FIG.2 BACKGROUND ART

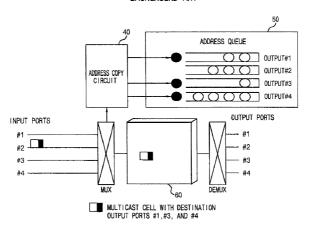
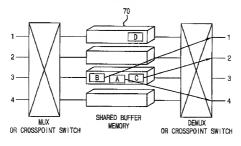


FIG.3
BACKGROUND ART



	ADDRESS QUEUE	]
OUTPUT PORT #1	B D	
OUTPUT PORT #2		IDLE STATE PRODUCES BY HOL BLOCKING
OUTPUT PORT #3		BY HUL BLUCKING
OUTPUT PORT #4	A	
TAIL	HEAD	

FIG.4

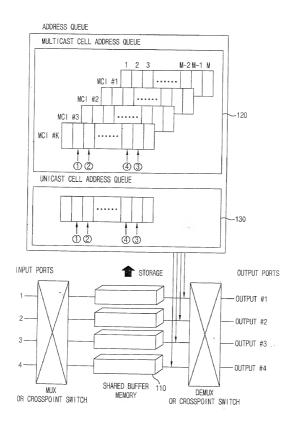
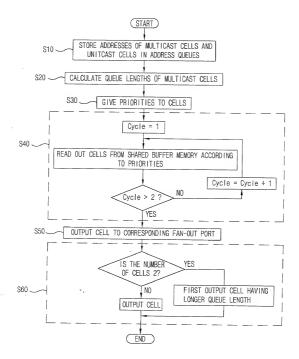


FIG.5



William Charles

FIG.6

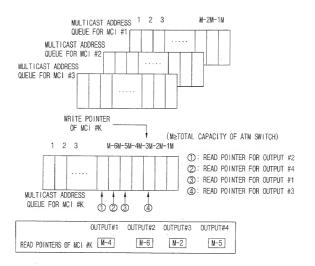


FIG.7A

	OUTPUT #1	OUTPUT #2	OUTPUT #3	OUTPUT #4
MCI #1 ADDRESS QUEUE	89	88	90	84
MCI #2 ADDRESS QUEUE	91	95	80	83
MAXIMUM QUEUE LENGTH	91	95	90	84
PRIORITY	2	1	3	4

FIG.7B

		OUTPUT PORT				
		1	2	3	4	
READ PRIORITY	1st			SBM #4(s <sub>1</sub> )		
	2nd	SBM #2(s <sub>2</sub> )				
	3rd		SBM #2(s <sub>3</sub> )			
	4th				SBM #2(\$4)	

OUTPUT PORT & READ PRIORITY OF UNICAST CELL(s)

FIG.7C

		-	OUTPUT PO	JKI -	
		_ 1	2	3	4
READ PRIORITY	1st		SBM #2(m <sub>1</sub> )		
	2nd	SBM #3(m <sub>2</sub> )			
	3rd			SBM #4(m <sub>3</sub> )	
	4th				SBM #4(m <sub>4</sub> )
				L	

QUEUE LENGTH OF m1 : 95 QUEUE LENGTH OF m2 : 91 QUEUE LENGTH OF m3 : 90 QUEUE LENGTH OF m4 : 84

OUTPUT PORT & READ PRIORITY OF MULTICAST CELL(m)

F1G.8

